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Re Applic of	Karl-Eugen Kroell et al.
Docket No.	DE920000026US1
Serial No.	09/902,140
Filing Date	July 10, 2001
Attorney	Steven Capella

Attached: APPEAL BRIEF *in triplicate*

PLEASE DELIVER TO:

EXAMINER: Hugh M. Jones
ART UNIT: 2123
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INTERNATIONAL BUSINESS MACHINES CORPORATION

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I hereby certify that this correspondence is being deposited by FACSIMILE to the Commissioner of Patents, PO Box 1450, Alexandria, VA 22313-1450 on February 10, 2004 by Colleen Dew.

Colleen J Dew

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2123

In re application of	:	February 10, 2004
Karl-Eugen Kroell et al.	:	Examiner: Hugh M. Jones
Serial No.: 09/902,140	:	
Filed: July 10, 2001	:	IBM Corporation Dept. 18G/Bldg. 300-482
Title: AUTOMATIC CHECK FOR CYCLIC OPERATING CONDITIONS FOR SOI CIRCUIT SIMULATION	:	2070 Route 52 Hopewell Junction, NY 12533-6531

APPEAL BRIEF

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final Rejection of claims 1, 2, 5-8, 13 and 14. A correct copy of the claims is attached in the Appendix.

Real Party in Interest

The real parties in interest is International Business Machines Corporation per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 011992/0452 on July 10, 2001.

Related Appeals and Interferences

None.

Status of Claims

Claims 1, 2, 5-8, 13 and 14 are pending.

Status of Amendments

No amendments after Final Rejection have been submitted.

Summary of Invention

The invention centers on the idea of performing a comparison of steady state DC conditions corresponding to the beginning and end of a test cycle (present claim 1 step (c)) and storing such information (present claim 1 step (d)) prior to performing any testing/simulation of transient response (present claim 8 step (f) and present claim 14, step (f)). In this manner, adjustments can be made either to the test conditions and/or to the device configuration prior to starting computation-intensive transient response analysis. See the specification at page 4, line 8-16 and Figure 1, reference numeral 130.

Issues

1. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the judicially created doctrine of obviousness-type double patenting over Joshi et al. (US Pat. 6,442,735) in view of Dangelo et al. (US Pat. 5,555,201).

2. Whether claims 1, 5, 7, 13 are patentable under 35 USC 102(e) over Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

3. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the 35 USC 102(e) over Joshi et al. (US Pat. 6,442,735).

4. Whether claims 1, 2, 5-8, 13 and 14 are patentable under 35 USC 103(a) over Sakamoto US Pat. 6,063,130) in view of (Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

Grouping of Claims

The claims stand or fall together within each respective issue identified above except for issues 1-3 where appellants submit that claims 8 and 14 are further separately patentable for the reasons stated below.

Argument

1. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the judicially created doctrine of obviousness-type double patenting over Joshi et al. (US Pat. 6,442,735) in view of Dangelo et al. (US Pat. 5,555,201).

Joshi et al. (US6442735) discloses an SOI circuit simulation method where "DC analysis" is performed prior to transient response simulation. The DC analysis of Joshi et al. appears to be an assessment relative to an initial DC condition. Joshi et al. does not disclose or suggest comparing device response to two different DC conditions as in present claim 1 step (c), nor storing any information based on such a comparison as in present claim 1 step (d). Joshi et al. does not disclose or suggest performing transient analysis after such comparison of DC conditions as in claim 8 step (f) and claim 14, step (f).

Dangello et al. (US 5555201) discloses techniques and systems for hierarchical display of control and dataflow information. Dangello et al. appears to be relied on for its disclosure concerning object-oriented displays. Dangello et

al. does not disclose or suggest anything regarding DC testing, much less comparing device response to two different DC conditions and storing any information based on such a comparison.

The combination of Joshi et al. and Dangello et al. would thus fail to provide for comparing device response to two different DC conditions as in present claim 1 step (c), nor storing any information based on such a comparison as in present claim 1 step (d).

Claims 8 and 14 are further separately patentable in as much as combination of Joshi et al. and Dangello et al. would fail to provide foe performing transient analysis after such comparison of DC conditions as in claim 8 step (f) and claim 14, step (f).

Appellants submit that the above arguments for patentability do not rely on unclaimed features. Thus, appellants submit that the present claims do not represent obviousness-type double patenting over Joshi et al. in view of Dangelo et al.

2. Whether claims 1, 5, 7, 13 are patentable under 35 USC 102(e) over Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

Wong (US Patent 4,918,643) describes a method of developing a linear vector description of system response over a cycle where the system is to be forced to steady state. Where the series of vectors does not result in a steady state at the end of the cycle, Wong changes the initial vector using a Jacobian matrix calculation. Since this method potentially involves multiple Jacobian matrix calculations, Wong describes an alternative method for computing the

Jacobian matrix. Wong compares the starting vector with the final vector to see if final vector is substantially the same as the starting vector. This final vector is the result of a transient calculation using the series of linear vectors described in Wong. Wong does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

Wong et al. (IEEE article) discloses a method of switching regulator analysis where the an open loop configuration is used to lessen the impact of the feedback circuitry in the case of a poor guess. Wong et al. performs a time domain simulation technique assuming a periodic network waveform and then iteratively runs the simulation until starting conditions are found which result in a steady state condition. Wong et al. does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong et al. does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

Claims 8 and 14 are further separately patentable over Wong and Wong et al. in as much as neither reference discloses or suggests performing transient analysis after manual correction as required by present claims 8 and 14.

3. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the 35 USC 102(e) over Joshi et al. (US Pat. 6,442,735).

Joshi et al. (US6442735) discloses an SOI circuit simulation method where "DC analysis" is performed prior to transient response simulation. The DC analysis of Joshi et al. appears to be an assessment relative to an initial DC condition. Joshi et al. does not disclose or suggest comparing device response

to two different DC conditions as in present claim 1 step (c), nor storing any information based on such a comparison as in present claim 1 step (d).

Claims 8 and 14 are further separately patentable over Joshi et al. in as much as Joshi et al. does not disclose or suggest performing transient analysis after such comparison of DC conditions as in claim 8 step (f) and claim 14, step (f).

For the above reasons, appellants submit that the claims are not anticipated by Joshi et al.

4. Whether claims 1, 2, 5-8, 13 and 14 are patentable under 35 USC 103(a) over Sakamoto US Pat. 6,063,130) in view of (Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

Sakamoto (US6063130) appears to employ a passivity check for linear circuit elements prior to transient response simulation. Sakamoto performs this passivity check by preparing and inductance matrix and checking the minor determinants. If the element is not passive, this result is reported back and the testing is aborted. Sakamoto does not give any apparent details regarding the DC analysis of figure 2, step 24. At best, this would appear to be a DC analysis of the cycle start condition. Sakamoto does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Sakamoto does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis.

Wong (US Patent 4,918,643) describes a method of developing a linear vector description of system response over a cycle where the system is to be forced to steady state. Where the series of vectors does not result in a steady state at the end of the cycle, Wong changes the initial vector using a Jacobian matrix calculation. Since this method potentially involves multiple Jacobian matrix calculations, Wong describes an alternative method for computing the Jacobian matrix. Wong compares the starting vector with the final vector to see if final vector is substantially the same as the starting vector. This final vector is the result of a transient calculation using the series of linear vectors described in Wong. Wong does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

Wong et al. (IEEE article) discloses a method of switching regulator analysis where the an open loop configuration is used to lessen the impact of the feedback circuitry in the case of a poor guess. Wong et al. performs a time domain simulation technique assuming a periodic network waveform and then iteratively runs the simulation until starting conditions are found which result in a steady state condition. Wong et al. does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong et al. does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

The combination of Sakamoto with the teaching of Wong or Wong et al. would not render the invention obvious in as much as the combined teaching of these references would not lead one of ordinary skilled in the art to perform the comparison of DC simulations and/or manual correction prior to transient analysis in response to such comparison as presently claimed.

Conclusion

Based on the above arguments, appellants submit that the present claims are patentable over the prior art of record that all the rejections should be reversed.

Respectfully submitted,
Karl-Eugen Kroell et al.

By _____
Steven Capella, Attorney
Reg. No. 33,086
Telephone: 845-894-3669

Appendix

Claims on Appeal

1. A method for simulating hardware circuits during which voltages are calculated at a plurality of circuit nodes, comprising the steps of:
   (a) carrying out a first DC-simulation run at the beginning of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

2. The method according to claim 1 further comprising the steps of:
   (e) outputting said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

5. The method according to claim 1 comprising the step of setting the START TIME prior to the begin of a functional cycle.

6. The method according to claim 1 in which the hardware is built according to silicon-on insulator (SOI) technology.

7. A computer system having installed program means comprising program code portions for performing the steps:
   (a) carrying out a first DC-simulation run at the beginning of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

8. The computer system according to claim 7 further comprising program code portions for performing the steps:
   (e) outputting said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

13. Computer program product stored on a computer-readable medium, said product comprising code that, when executed, causes a computer to perform the method comprising:

(a) carrying out a first DC-simulation run at the beginning of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

14. The computer program product according to claim 13 wherein said method further comprises performing the steps:

(e) outputting said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. DE920000026US1

In Re Application Of: **Karl-Eugen Kroell et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/902,140	July 10, 2001	Hugh M. Jones	2123

Invention:

AUTOMATIC CHECK FOR CYCLIC OPERATING CONDITIONS FOR SOI CIRCUIT SIMULATION

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

The fee for filing this Appeal Brief is: **$330.00**

☐ A check in the amount of the fee is enclosed.

The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **09-0458,FI-035**

Steven Capella

Signature

Dated: **February 10, 2004**

Steven Capella, Registration No. 33,086
International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533
845-894-3669

I certify that this document and fee is being faxed on **Feb. 9, 2004**
and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Colleen J. Dew

Signature of Person Faxing Correspondence

Colleen J. Dew

Typed or Printed Name of Person Faxing Correspondence

cc:

I hereby certify that this correspondence is being deposited by FACSIMILE to the Commissioner of Patents, PO Box 1450, Alexandria, VA 22313-1450 on February 10, 2004 by Colleen Dew.

Colleen J. Dew

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2123

In re application of	:	February 10, 2004
Karl-Eugen Kroell et al.	:	Examiner: Hugh M. Jones
Serial No. : 09/902,140	:	
Filed: July 10, 2001	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: AUTOMATIC CHECK FOR CYCLIC OPERATING CONDITIONS FOR SOI CIRCUIT SIMULATION	:	2070 Route 52 Hopewell Junction, NY 12533-6531

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Commissioner for Patents
Alexandria, VA 22313-1450

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Related Appeals and Interferences

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Summary of Invention

The invention centers on the idea of performing a comparison of steady state DC conditions corresponding to the beginning and end of a test cycle (present claim 1 step (c)) and storing such information (present claim 1 step (d)) prior to performing any testing/simulation of transient response (present claim 8 step (f) and present claim 14, step (f)). In this manner, adjustments can be made either to the test conditions and/or to the device configuration prior to starting computation-intensive transient response analysis. See the specification at page 4, line 8-16 and Figure 1, reference numeral 130.

Issues

1. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the judicially created doctrine of obviousness-type double patenting over Joshi et al. (US Pat. 6,442,735) in view of Dangelo et al. (US Pat. 5,555,201).

2. Whether claims 1, 5, 7, 13 are patentable under 35 USC 102(e) over Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

3. Whether claims 1, 2, 5-8, 13 and 14 are patentable under the 35 USC 102(e) over Joshi et al. (US Pat. 6,442,735).

4. Whether claims 1, 2, 5-8, 13 and 14 are patentable under 35 USC 103(a) over Sakamoto US Pat. 6,063,130) in view of (Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

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Dangello et al. (US 5555201) discloses techniques and systems for hierarchical display of control and dataflow information. Dangello et al. appears to be relied on for its disclosure concerning object-oriented displays. Dangello et

al. does not disclose or suggest anything regarding DC testing, much less comparing device response to two different DC conditions and storing any information based on such a comparison.

The combination of Joshi et al. and Dangello et al. would thus fail to provide for comparing device response to two different DC conditions as in present claim 1 step (c), nor storing any information based on such a comparison as in present claim 1 step (d).

Claims 8 and 14 are further separately patentable in as much as combination of Joshi et al. and Dangello et al. would fail to provide foe performing transient analysis after such comparison of DC conditions as in claim 8 step (f) and claim 14, step (f).

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2. Whether claims 1, 5, 7, 13 are patentable under 35 USC 102(e) over Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

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Jacobian matrix. Wong compares the starting vector with the final vector to see if final vector is substantially the same as the starting vector. This final vector is the result of a transient calculation using the series of linear vectors described in Wong. Wong does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

Wong et al. (IEEE article) discloses a method of switching regulator analysis where the an open loop configuration is used to lessen the impact of the feedback circuitry in the case of a poor guess. Wong et al. performs a time domain simulation technique assuming a periodic network waveform and then iteratively runs the simulation until starting conditions are found which result in a steady state condition. Wong et al. does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong et al. does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

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Joshi et al. (US6442735) discloses an SOI circuit simulation method where "DC analysis" is performed prior to transient response simulation. The DC analysis of Joshi et al. appears to be an assessment relative to an initial DC condition. Joshi et al. does not disclose or suggest comparing device response

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For the above reasons, appellants submit that the claims are not anticipated by Joshi et al.

4. Whether claims 1, 2, 5-8, 13 and 14 are patentable under 35 USC 103(a) over Sakamoto US Pat. 6,063,130) in view of (Wong (US Pat. 4,918,643) or Wong et al. (IEEE - 1997 article "Accelerated Steady-State Analysis ...").

Sakamoto (US6063130) appears to employ a passivity check for linear circuit elements prior to transient response simulation. Sakamoto performs this passivity check by preparing and inductance matrix and checking the minor determinants. If the element is not passive, this result is reported back and the testing is aborted. Sakamoto does not give any apparent details regarding the DC analysis of figure 2, step 24. At best, this would appear to be a DC analysis of the cycle start condition. Sakamoto does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Sakamoto does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis.

Wong (US Patent 4,918,643) describes a method of developing a linear vector description of system response over a cycle where the system is to be forced to steady state. Where the series of vectors does not result in a steady state at the end of the cycle, Wong changes the initial vector using a Jacobian matrix calculation. Since this method potentially involves multiple Jacobian matrix calculations, Wong describes an alternative method for computing the Jacobian matrix. Wong compares the starting vector with the final vector to see if final vector is substantially the same as the starting vector. This final vector is the result of a transient calculation using the series of linear vectors described in Wong. Wong does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

Wong et al. (IEEE article) discloses a method of switching regulator analysis where the an open loop configuration is used to lessen the impact of the feedback circuitry in the case of a poor guess. Wong et al. performs a time domain simulation technique assuming a periodic network waveform and then iteratively runs the simulation until starting conditions are found which result in a steady state condition. Wong et al. does not do a DC simulation of end of cycle conditions as required by the present claims. Appellants submit that Wong et al. does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop.

The combination of Sakamoto with the teaching of Wong or Wong et al. would not render the invention obvious in as much as the combined teaching of these references would not lead one of ordinary skilled in the art to perform the comparison of DC simulations and/or manual correction prior to transient analysis in response to such comparison as presently claimed.

Conclusion

Based on the above arguments, appellants submit that the present claims are patentable over the prior art of record that all the rejections should be reversed.

Respectfully submitted,
Karl-Eugen Kroell et al.

By _____
Steven Capella, Attorney
Reg. No. 33,086
Telephone: 845-894-3669

Appendix

Claims on Appeal

1. A method for simulating hardware circuits during which voltages are calculated at a plurality of circuit nodes, comprising the steps of:
   (a) carrying out a first DC-simulation run at the beginning of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

2. The method according to claim 1 further comprising the steps of:
   (e) outputting said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

5. The method according to claim 1 comprising the step of setting the START TIME prior to the begin of a functional cycle.

6. The method according to claim 1 in which the hardware is built according to silicon-on insulator (SOI) technology.

7. A computer system having installed program means comprising program code portions for performing the steps:
   (a) carrying out a first DC-simulation run at the beginning of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

8. The computer system according to claim 7 further comprising program code portions for performing the steps:
   (e) outputting said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

13. Computer program product stored on a computer-readable medium, said product comprising code that, when executed, causes a computer to perform the method comprising:

(a) carrying out a first DC-simulation run at the beginning of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

14. The computer program product according to claim 13 wherein said method further comprises performing the steps:

(e) outputting said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

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